METHOD FOR DESIGNING CLOCK WIRING CIRCUIT OF SEMICONDUCTOR INTEGRATED CIRCUIT

Patent Number: JP8044776
Publication date: 1996-02-16
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Requested Patent: JP8044776
Application Number: JP19940178325 19940729
Priority Number(s):
IPC Classification: G06F17/50
EC Classification:
Equivalents:

Abstract

PURPOSE:To obtain improvement which suppresses clock skew as the time difference of a clock signal applied to a circuit element.
CONSTITUTION:As for the designing method for the clock wiring circuit of the semiconductor integrated circuit which designs logic, designs layout next, and arranges clock buffers 2 in a tree shape, a clock circuit at the time of the logic designing is not provided with the clock buffers 2, but provided with only an I/O input buffer 1, which is connected directly to a circuit element 3 which requires a clock signal; when the layout is designed, the clock buffers 2 determined by the number of circuit elements 3 requiring the clock signal are arranged in the tree shape as clock circuits, and a clock wiring branch pattern 5 is so arranged that the delay time of a clock wiring trunk pattern 4 approximates the delay time excluding the wiring delay time of a clock signal wire estimated from the overall area of the semiconductor integrated circuit.